

Brenda L. Luderman (bluderman@gmail.com)

Cell: 940-206-0844

Extended CV: www.brendaluderman.info/cv

GOALS

Advance and continue my career as a SoC Power Grid Designer, SRAM, Flash, DRAM, Non-Volatile Memory Designer, Fast Spice/Mixed-Mode Verification/EDA Engineer or Custom/Mixed-Signal Designer. Recently moved to DFW to join spouse.

EXPERIENCE

12 years, as a Senior Circuit Designer and a PhD EE, for two Fortune 500 Companies. I have contributed to the success of three generations of Application Processors and the development of Flash, DRAM and SRAM for low power 65nm, 90nm, 0.18um, 0.25um and 0.4um CMOS technologies.

EDUCATION

PhD Electrical Engineering May '94. MS EE '89, BS EE'88. University of Rochester, Rochester, NY.

SKILLS

Custom IC and Memory Design, Full-Chip Multi-VDD Power Delivery, Mixed Digital/Analog Circuit Design, CAD/EDA Experience with Cadence, Mentor Graphics, Synopsys, Magma, OEA and Hardware/Software Programming in Verilog, Perl, Ruby and C.

TECHNICAL ACCOMPLISHMENTS

1. SoC Power Grid Designer and EDA, Intel.

6/03– 6/06.

Senior circuit designer responsible for power grid design, power switches, grid implementation spec, pre-layout IR drop simulations, managing 170GB of project lef, def, spf and trans data for post-layout static IR drop simulations and silicon validation, PXA320. Tools: Spice, Pplan/Pgrid, Voltagestorm, Composer, Virtuoso, Magma, Synopsys, Calibre.

2. SRAM Memory Designer, Intel.

7/00 – 5/03.

Senior project leader responsible for module specification, circuit design, schematics, spice and fast spice simulation verification and post-silicon IMS testing of 256KB 0.18um SRAM module, PXA27x. Tools: Spice, Composer, Virtuoso, Modelsim, HSIM, Hercules.

3. Flash Memory Designer, Motorola.

6/98 – 7/00.

Team leader responsible for project planning, design and task delegation, analog test modes, specifying schematic libraries and reviewing spice models on a 1Mb 0.25um 1.5T Embedded Flash Memory. Tools: Spice, Composer, Virtuoso.

4. DRAM Memory Designer, Motorola.

10/96 – 5/98.

Technical leader responsible for module specification, test implementation guide, circuit design, verification and post-silicon characterization of a 256Kb 0.4um Embedded BST DRAM. Tools: Spice, Design Architect, IC Station, Hercules.

5. Fast Spice/Mixed Mode Design Verification and EDA. Intel

Volunteered and helped fast spice/mixed-mode simulation team complete verification tasks. Using extracted spice netlist and Verilog VCD input, simulated mixed-signal behavior of the PXA320 768KB SRAM and the PXA27x 128KB SRAM islands with HSIM. Using Mixed-Mode ADVMS simulations, compared Verilog and Spice results for selected circuits found in a Services macro, PXA320. Tools: HSIM, Modelsim, Mentor's ADVMS.

CAREER OVERVIEW

1. Intel, Applications Processors (now Marvell). Senior Circuit Designer. Austin, TX.

7/00 – 7/07.

2. Motorola, Semiconductor Products (now Freescale). Senior Scientist. Austin, TX.

8/94– 7/00.